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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,693	07/29/2004	Rishi BHOOSHAN	TI-37087	4692

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
06/14/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,693	BHOOSHAN ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *13-24 and 37-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 25-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's arguments filed on 10/03/2006. Claims 1-48 are pending, wherein claims 13-24,37-48 are withdrawn from consideration as being directed to non-elected inventions without traverse, as previously indicated.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-8,25-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Itazu et al.** (U.S. Patent No. 6,405,354) in view of **Fujine** (US Patent Application Publication No. 2002/0199160).

As per **claims 1,25**, **Itazu et al.** disclose the elements of the claims as illustrated in Figs. 5-6, wherein the extraction of the topology of the design are performed in steps S1 to S10 (see also col. 5, line 11 to col. 6, line 39) wherein the power network includes resistors and the temporary cells include transistors (see col. 1, lines 32-44; col. 6, lines 40-48); wherein the model generation including replacing the transistors (i.e., temporary cells) with current source and computing the magnitude of the current sources are further described in steps S11 to S14 (see col. 6, line 40 to col. 7, line 6) wherein since the resistances and current sources are based in part on the width or size of the wirings

and/or transistors (col. 6, lines 40-48; col. 5, lines 23-33; col. 8, lines 24-33), the magnitude of the current sources are accordingly correspond to some proportion of the width of the wirings and/or transistors; wherein the analysis including the determination if the design violates the desired criteria are further described in steps S15 to S16 (col. 7, lines 7-23); wherein the computer readable medium carrying one or more sequences of instructions for performing these steps are further described in col. 2, lines 60-65 (see also col. 4, line 55 to col. 5, line 6). However, **Itazu et al.** fails to specifically requires that all transistors be replaced with the current sources or that the temporary cells are in units of transistors which are then replaced with current sources, from which the model is generated. **Fujine** teaches a method/system for analyzing power supply network in which all circuit elements, such as functional blocks, transistors, and logic gates, are replaced with current sources in order to accurately and quickly evaluate whether there is sufficient power to ensure the operation of the individual circuits (see paragraphs [0041], [004], [0009]). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further modify the teachings of **Itazu et al.** so that all circuit elements including all transistors are replaced with current sources as taught by **Fujine** because such modifications would further allows for both accuracy and efficiency in evaluating power supply networks.

As per **claims 2-3,5,26-27,29**, **Itazu et al.** in view of **Fujine** teaches all of the elements of claims 1,25, from which the respective claims depend, are discussed in the rejection of claims 1,25 above, wherein the further criteria of using the current density and supply voltage drop to ensure that they do not exceed the desired amount are

described in **Itazu et al.**, col. 7, lines 7-23, wherein such maximum values (i.e., standard values) are further described in **Itazu et al.**, col. 1, line 54 to col. 2, line 7; wherein such cells or modules are rejected when a re-layout is executed.

As per **claims 4,28**, **Itazu et al.** in view of **Fujine** teach all of the elements of claims 3,27, from which the respective claims depend, are discussed in the rejection of claims 3,27 above, wherein the treatment of the transistors being connected parallel are illustrated in **Itazu et al.**, Figs. 2 and 15 in which the current sources, representing the transistors, are analyzed as being connected in parallel.

As per **claims 6,30**, **Itazu et al.** in view of **Fujine** teach all of the elements of claims 5,29, from which the respective claims depend, are discussed in the rejections of claims 5,29 above, wherein since the "modules" comprises many cells and wirings, the analysis of the modules are accordingly performed at a higher level (i.e., chip-level analysis).

As per **claims 7,31**, **Itazu et al.** in view of **Fujine** teach all of the elements of claims 6,30, from which the respective claims depend, are discussed in the rejections of claims 6,30 above, wherein since the models are generated based estimated values and extraction values (see **Itazu et al.**, col. 6, lines 40-67), such models are accordingly performed using some sort of simulation tool.

As per **claims 8,32**, **Itazu et al.** in view of **Fujine** teach all of the elements of claims 3,27, from which the respective claims depend, are discussed in the rejections of claims 3,27 above, wherein such layout file would necessarily be provided in order to

store the particular cell arrangements/interconnections of the circuit layout for the analysis (see **Itazu et al.**, col. 5, line 10 to col. 6, line 35).

4. **Claims 9-12,33-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Itazu et al.** (U.S. Patent No. 6,405,354) in view of **Fujine** (US Patent Application Publication No. 2002/0199160) and **Djaja et al.**(U.S. Patent No. 6,405,160).

As per **claims 9-12,33-36**, **Itazu et al.** in view of **Fujine** disclose all of the elements of claims 1,25, from which the respective claims depend, as discussed in the rejections of claims 1,25 above. However, **Itazu et al.** in view of **Fujine** failed to particular apply such circuit design analysis of the chip-level design comprising transistors and resistors to memory circuits, involving the particular memory array with row arrangements as claimed. **Djaja et al.** disclose a method/system for designing memory array having row arrangements (see col. 2, line 41 to col. 3, line 12) which takes into account current density, and further make use of locations/coordinates of transistors to keep track of the critical features of the device layout (see col. 4, lines 8-55). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further adapt the method/system of **Itazu et al.** in view of **Fujine** to analyze the memory array circuits as taught by **Djaja et al.** because such adaptation would allow the particular memory circuits as taught by **Djaja et al.** to be verified for proper functionality.

Remarks

5. As per **claims 1-12,25-36**, Applicant argued that the references, including **Fujine**, fail to teach or suggest replacing each transistor with a corresponding current source, wherein **Fujine** only discloses that "circuit elements, such as transistors, logic gates and functional blocks, are converted to current sources based on design information stored in the design information storage means". Also, Applicant argued that the references do not show, teach, or suggest "computing a magnitude of each of said plurality of current sources by distributing an aggregate amount of current sunk by said module among said plurality of current sources". The Examiner is not persuaded. First of all, since **Fujine** teaches the "circuit elements" as recited by Applicant, comprise transistors, which are then converted to current sources, all of these transistors corresponding to the circuit elements, would in effect be "replaced" with corresponding current sources, in order to accurately and quickly evaluate whether there is sufficient power to ensure the operation of the individual circuits, making it obvious to one of ordinary skilled in the art at the time of the invention to incorporate this teaching of **Fujine** into the method/system of **Itazu et al.** so as to require that all transistors of **Itazu et al.** be replaced with current sources to evaluate the circuit operations, for the reasons given above. Accordingly, the plurality of these current sources resulting from such replacement, are taken into account as part of teaching of **Itazu et al.** in computing of magnitude of each of the plurality of current sources as discussed in the rejections above (see col. 6, line 40 to col. 7, line 6).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

/Phallaka Kik/
Primary Examiner, A.U. 2825
June 3, 2007